Notice of Allowability	Application No.	Applicant(s)	
	10/670,716	LUICK, DAVID A.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *22 March 2007*.

2. ☒ The allowed claim(s) is/are *1 and 3-17*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GABRIEL CHU
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Bryan W. Bockhop on 7 May 2007.

The application has been amended as follows:

Claim 1 is amended, ""A runtime repairable processor within a single silicon chip, comprising:

a first data path of a plurality of data paths [[that are contained]], said first data path defining [[on]] a first area on the silicon chip by its wire width;

a plurality of data registers disposed on the silicon chip and coupled to the plurality of data paths;

a first functional unit comprising a plurality of bit-level operational units [[disposed]] on [[the first area of]] the silicon chip and coupled to the plurality of data paths;

[[a second area on the silicon chip that is a portion of the first area and smaller that the first are, the second area incapable of receiving thereon a functional unit that would require a data path that is different from the plurality of data paths;]]

a second functional unit that is a duplicate of the first functional unit, said second functional unit comprising a plurality of duplicate bit-level operational units, and that is

disposed on [[the second area of]] the silicon chip, the second functional unit coupled to the plurality of data paths, wherein a first bit-level operational unit of the first functional unit and a first duplicate bit-level operational unit of the second functional unit are both contained within the first area; and

an enabling control logic that is configured to disable the first functional unit and to enable the second functional unit when a failure is detected with the first functional unit.

Claim 11 is amended, "A method for providing a fault tolerant computing runtime repairable processor on a single silicon chip, comprising the steps of:

connecting a plurality of data registers to a first functional unit comprising a plurality of bit-level operational units through a plurality of data paths, wherein [[the plurality of data paths that are contained on]] a first area of the silicon chip is defined by the wire width of a first datapath of the plurality of data paths, the plurality of data registers and the first functional unit disposed on [[the first area of]] the silicon chip;

placing a second functional unit, that is a duplicate of the first functional unit comprising a plurality of duplicate bit-level operational units, [[on a second area]] on the silicon chip[[that is a portion of the first area and that is smaller than and included in the first area, wherein the second area is incapable of receiving thereon a functional unit that would require a data path that is different from the plurality of data paths]], wherein a first bit-level operational unit of the first functional unit and a first duplicate bit-level operational unit of the second functional unit are both contained within the first area;

connecting the plurality of data registers to the second functional unit through the plurality of data paths;

detecting an error condition in the first functional unit;

in response to detecting the error condition, disabling the first functional unit and enabling the second functional computing unit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gabriel L. Chu
Primary Examiner
Art Unit 2114

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